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(71) Applicant *(for all designated States except US)*: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S-126 25 Stockholm (SE).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: JARSTAD, Tomas [SE/SE]; Skälbyvägen 24E, S-191 49 Sollentuna (SE). NORSTRÖM, Hans [SE/SE]; Mårdstigen 3, S-171 72 Solna (SE).

(74) Agents: LARFELDT, Helene et al.; Bergenstråhle & Lindvall AB, P.O. Box 17704, S-118 93 Stockholm (SE).

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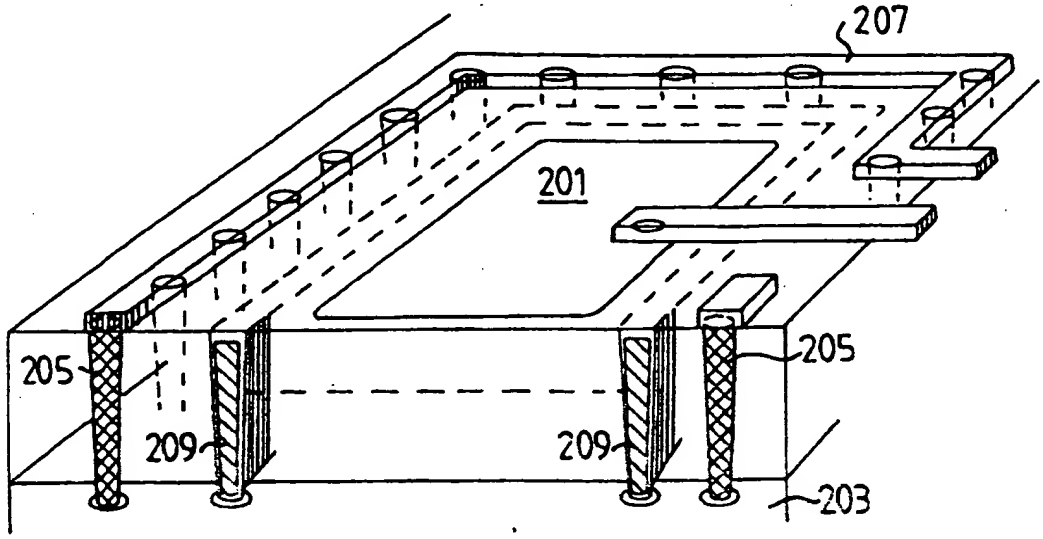

(57) Abstract

Low-resistant contacts (205) are made from the surface of a semiconductor component (201), down into the substrate (203) thereof by means of etching a hole down into the substrate (203), which then, for example, by means of CVD deposition is filled with a metal e.g. tungsten. Moreover, by further locating such substrate contacts at clos distances around a component (201) or a block or a group o components, a very good electrical shielding against other components or blocks of components located on the same substrate is obtained Shielding can also be obtained vertically upwards by means of applying a metal layer on top of the component. The metal plugs obtained in this manner can also be used for lateral shielding of electrical signal conductors in a semiconductor structure.

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SEMICONDUCTOR DEVICE SHIELDED BY AN ARRAY OF ELECTRICALLY CONDUCTING PINS AND A METHOD TO MANUFACTURE SUCH A DEVICE

TECHNICAL FIELD

The present invention relates to devices, in particular substrate contacts and shielding devices, in a semiconductor component and methods of manufacturing these. Furthermore, the invention relates to a method of arranging substrate contacts.

BACKGROUND OF THE INVENTION AND PRIOR ART

In manufacturing silicon components being densely packed it is of great importance to avoid undesired coupling between different blocks of components located on the same silicon substrate. Such an undesired coupling or "cross-talk" between different blocks is most often more inconvenient in the manufacturing of analogue digital integrated circuits (IC) of a so called mixed-mode type. Cross-talk between different circuit blocks can either take place via capacitive coupling between the connection conductors or via substrate coupling. A number of different approaches for minimizing cross-talk, via the substrate, are described in literature, see for example K. Joardar; "A simple approach to modeling cross-talk in integrated circuits", IEEE J. Solid State Circuits. vol. 29, 1994, pp. 1212.

It is characteristic of all described techniques that different types of isolation methods in combination with substrate contacts for suppressing cross-talk are used. In addition to having good isolation between the respective blocks it is also required that the subtract contact is made as low-resistant as possible in order to achieve the best possible result.

The drawback with the methods described in the paper mentioned above, is that the contact resistance between the metal and substrate becomes comparatively high, since doped silicon, a P-plug, is used as connection. Said diffusion of a P-type must also be made having a depth of several μm in order to secure contact between a high-doped substrate and metal. This requires a long drive-in diffusion time in combination with a high drive-in diffusion temperature which is not desirable in the

manufacturing of modern compon nts where a low temperature budget is aimed at. Last but not least, the P^+-diffusion, i.e. the so called guard-ring, is space demanding, since lateral diffusion takes place simultaneously with the vertical diffusion.

SUMMARY

It is an object of the present invention to provide a low-resistant substrate contact for semiconductor components which overcomes the drawbacks arising when forming substrate contacts according to prior art.

It is further an object of the present invention to provide a method of locating and arranging these substrate contacts around a component or a block of components in order to obtain a good shielding between different components or blocks of components.

These and other objects are obtained using a substrate contact made of metal, extending deep down into the underlying semiconductor material, all the way down into the substrate. Furthermore, by means of locating several such metallic substrate contacts at close intervals around components or blocks of components effective shielding towards undesired coupling or cross-talk is achieved.

Thus, a semiconductor component is obtained in a usual manner by means of using different substructures at and/or on a surface of a substrate. There is an electrical connection in the shape of a plug of a material with good electrical conductivity between the substrate and the surface at and/or next to the semiconductor component. The material can be of another type than the substrate, which typically is semiconductive and can have different types of doping. The plug is preferably a metal plug and in any case extends from an inner part of the substrat to an area close to the surface next to or at the semiconductor component. Furthermore, the plug should xtend deeper down into the substrate than into the PN-junctions introduced and/or existing in the substrate. Several such plugs are preferably arranged around the surface of the semiconductor component and

can then serve as electrical shielding of the semiconductor component. Furthermore, the upper ends of the plugs are preferably electrically connected as by means of layers or paths of an electrically conducting material, which as above can be a material with good electrical conductivity, in particular a metal material.

In the manufacturing of the plugs, suitably shaped holes are first made and which then are filled with the electrically conducting material.

The filling is preferably provided at the same time as other contact holes for electrical contact with different electrod s in the semiconductor are filled. Holes can then be made having a diameter or largest across corner dimension, which essentially corresponds to the corresponding measures for the contact holes. In any event the diameters of the holes should be chosen so that they are completely filled in the process step for filling the contact holes.

Plugs of the above mentioned kind can also be arranged alongside a shielded electrical signal conductor in a semiconductor structure. The plugs must be arranged so close as to obtain a good lateral shielding of the electrical signal conductor. Shielding in a vertical direction can be achieved by means of suitable metal planes below and/or above the signal conductor, which can be manufactured at the same time as other metal planes in the semiconductor structure. The plugs are preferably in electrical connection with these metal planes.

DESCRIPTION OF THE DRAWINGS

The invention will now be described by way of non-limiting examples and with reference to the appended drawings, in which:

- Figure 1a-1c show different steps carried out in the manufacturing of a substrate contact.
- Figure 2 is an overall view showing a number of substrate contacts arranged in order to shield a component.
- Figure 3 shows a shielded signal conductor.
- Figure 4 is an overall view of a number of components arranged

on the same substrate.
- Figure 5 is a cross-section showing lat ral shielding obtained by means of substrate contacts in combination with a vertically shielding upper metal layer.

DESCRIPTION OF PREFERRED EMBODIMENTS

In figures 1a-1c different stages in the manufacturing of a substrate contact are shown. The figures show the manufacturing of a substrate contact in a rudimentary NMOS-process flow. Another application area in which the manufacturing is of particular importance is in the manufacturing of bipolar components for radio purposes. Moreover, different variations of the method can be used in the manufacturing of CMOS-components and bipolar components.

Figure 1a shows the active areas defined by for example LOCOS (LOCal Oxidation of Silicon) on a silicon substrate 101, where the substrate also can be made of other semiconductor materials such as for example, germanium, gallium arsenide, silicon carbide, indium phosphide. On top of the silicon substrate an epitaxial layer of silicon 103 has been grown, which typically is 5-10 μm thick. The figure also shows the remaining layer of field oxide 102.

Thereupon, see figure 1b, a thin gate oxide is thermally grown, and whereupon a coating of polysilicon 105, which can be heavily doped with a doping of N-type, in order to form the gate, takes place. The gate is defined by means of lithography and dry etching. Implantation, with e.g. arsenic or phosphor, and drive-in diffusion of the source-/drain areas 107, is carried out in a self-aligned manner after etching of the gate.

Next, a passivation layer 109 and possibly a future hard mask 111 of preferably silicon nitride and/or oxide are deposited, whereupon a lay r of photo resist 112 is applied on the wafer. The layer is then lith graphically patterned in ord r to define the substrate contacts which might be located in the shape f a frame of discreet contacts around the whole r parts of the component. The latter is analogue with the so called P^+-guard-

ring described in the above cited paper.

The resist pattern having openings of about 1 μm is then by means of dry etching transferred to the hard mask and the oxide layers, in this case a combination of the deposited passivation layer and the thermally grown field oxide. The photo resist is removed from the wafer, followed by an anisotrophic silicon etch. The anisotrophic silicon etch is made so deep, typically several μm, so that it reaches down into the underlying high-doped P^+-substrate. After completed etching possible etch remainings such as polymers and other impurities are removed by means of a combination of dry cleaning (plasma-strip) and wet chemical cleaning. The structure after these steps is shown in figure 1b.

Photo resist is then again applied on the wafer which is then contact hole patterned and etched. The wafer is cleaned after the contact hole etching, whereby resist remains and other organic impurities are removed with the combination of dry cleaning (plasma strip) and wet chemical cleaning. After etching off the possible hard mask and common wet chemical cleaning, the process proceeds according to previously well-known technique. However, a substrate contact etching is accomplished, etched both through the oxide passivation and deep down into the silicon, approximately 5 μm or at least deeper than the deepest PN-junctions. In ordinary contact hole etching it is however a requirement that the etch is stopped at the silicon surface, and thus only goes through the passivation, in order for the component to work.

As is shown i figure 1c a thin layer, such as having a thickness of about 1000 A.U. of a contact metal 113 of for example titanium, platinum or cobalt for contacting is then deposited, for example by means of coherent sputtering, such as ionised metal plasma (IMP) or physical polymering, which later can be silicidized. In immediate connection, another thin metal layer 115, for example having a thickness of about 500 A.U., is deposited by means of for example reactive sputtering or CVD-technique. This so called diffusion barrier which preferably is

made of titanium nitride is deposit d on the wafer, since it is then desired that the contact holes are conformally filled with a metal, pref rably tungsten, by means of CVD-technique. In order to secure a good metallurgical connection with the silicon wafer, said contact metal can be brought to be alloyed with th silicon at an elevated temperature, whereby a silicide can be created in the contact area as indicated above. After depositing the contact metal and the barrier, the contact metal is hence silicidized by means of RTP (Rapid Thermal Processing), or alternatively by means of a traditional oven process.

After the contact formation e.g. tungsten is deposited by means of CVD-technique over the wafer. The CVD-coating is conformally executed, whereby both the contact holes 119 and the substrate contacts 117 will be overgrown (plugged), if the thickness of the deposited metal layer is of the same magnitude as the contact hole dimension. Ordinary metallisation and patterning of the same for connection of the different components to a circuit terminate the process. The result is shown in figure 1c.

The metal plugs can also be located at locations not having a field oxide layer 102 as is shown by the metal plug 120.

By using the method described above, a metallic, low-resistant connection with the substrate is obtained. Said metallic substrate contacts may also serve as a shielding cage, a screening cage, around respective component or block of components. Hereby a unique possibility for suppressing cross-talk is provided.

As an alternative to the above described embodiments, for example a uniformly doped, P^-- or N^--silicon substrate may be used in the same manner as the P^+/P^--epi-material described above. If such a uniformly low-doped material is used, an xtra diffusion, i.e. doping, in the bottom of the substrate contacts should however be made in order to secure a low contact resistance.

The above described embodiment results in low-resistant metal

contacts to the substrate which have a considerably better performance than the earlier substrate contacts obtained by means of diffusion. In certain cases also doped polysilicon may constitute and serve as the contact to the substrate. In the two latter cases a substantially higher resistance is however obtained. The method of making holes down into the inner of the substrate and then fill this with a conducting material, metal, polysilicon, etc. is easily implemented in existing CMOS and or bipolar flows. Only one additional mask step together with the following anisotrophic silicon etching are added.

The substrate contacts which typically are round 6 μm deep are simultaneously filled with the other standard contacts which are around 1 μm deep, the filling being made by means of for example CVD-tungsten. Also other metals, for example Al, Cu, etc. which are possible to deposit by means of CVD-technique should work in a similar manner.

The fact that the contact resistance between metal and substrate becomes relatively low, since metal is used as connection constitutes further advantages. Furthermore, an attained low temperature budget can be kept. Last but not least the method is much less space demanding than the traditional technique, since no lateral diffusion takes place. The method is furthermore elegant in the sense that the substrate contacts and the usual contacts are filled at the same time. Thus, the filling requires no extra process step.

Moreover, the deep metal contacts of the substrate can be located so closely, that the component or the components, blocks or modules of components, behave as if they were placed in a close screening cage providing a maximal electrical shielding. Thus, the method provides a unique possibility for electrical shielding at component level.

In figure 2, a semiconductor component which has been shielded according to this principle is shown. Thus, a component, or a block of components 201, is shown on top of a substrate 203. Around this component or this block of components a large number

of holes have been made which extend deep down into the substrate 203 and these holes have subsequently been filled with metal in the above described manner in order to form metal plugs 205. These metal plugs 205 are further connected to a conducting material 207, which connects the upper parts of the metal plug 205. The deep substrate contacts can furthermore easily be combined with traditional trench-isolation 209 in order to obtain maximal isolation in combination with good shielding, which is a requirement in the manufacturing of advanced integrated circuits for radio applications.

The obtained substrate contact can also be used in order to laterally shield an electrical signal conductor in a semiconductor structure. This is obtained by means of providing metal plugs manufactured in the above described manner next to, on both sides of, an electrical signal conductor. The electrical signal conductor can also preferably be shielded in the vertical direction in a conventional manner by means of metal planes.

In figure 3, a conductor 301 in a semiconductor structure shielded according to this principle is shown. The conductor 301 is here arranged between two metal planes 303 and 305, respectively, one above and one below, shielding the conductor in a vertical direction. Furthermore, a number of holes have been made on both sides of the conductor, which reach down to the lower metal plane 305 and which are filled with a metal. The metal plugs 307 obtained in this manner shield the conductor in the lateral direction if they are placed close enough. The top ends of the metal plugs may also, like the material 207 shown in figure 2, be connected to an electrically conductive material, not shown.

Furthermore, figure 4 shows an overall view of two groups of semiconductor components 401 and 403, arranged on a common substrate, shielded from each other and the environment by means of the above described substrate contact 405. The substrate contacts 405 are in this embodiment arranged in triple rows around the component groups. The purpose of this is to obtain an even better shielding. Furthermore, signal conductors may in

this embodiment be arranged between some of the rows of the substrate contacts 405, wh reby also the signal conductors become shielded in accordance with the above. The substrate contacts are further formed with an essentially quadratic cross-section and the spacing between the plugs in a row can, for example, be between 50 and 100% of the thickness of the plugs.

Finally, in figure 5 it is shown how components and blocks of components can be shielded from each other by means of the above described substrate contacts in combination with a metal plane applied on top of the components. Thus, figure 5 shows a silicon substrate 501 on which a number of components have been arranged. The components are in this case shielded from each other laterally both by means of conventional trenches 503 filled with isolating polysilicon and also by means of metal substrate contacts 505 of tungsten made according to the above, going deep down into the substrate.

Furthermore, there is an additional metal layer 509 provided on top of the uppermost layer of passivation oxide 507, which is connected to ground. The purpose of this metal layer is to provide a vertical shielding upwards of the components provided on the substrate. In this manner a screening cage for electrical shielding around the components is obtained.

The shielding layer of metal 509 does not need to be closed, it only needs to be arranged to cover such a large part of the top side of the components required to obtain a good vertical electrical upwards shielding. On the contrary it may be advantageous to provide perforations or holes 511 in the metal layer, which act in order to prevent or lower the risk for the metal to come loose.

CLAIMS

1. A semiconductor component arranged at a surface of a substrate comprising an electrical connection between the substrate and the surface on and/or at the semiconductor component, **characterized in** that the connection comprises a plug of a material having good electrical conductivity in particular a material of another type than the substrate, in particular a metal plug, which extends between the inner of the substrate and the surface layer at or on the semiconductor component.

2. A component according to claim 1, **characterized in** that the plug extends deeper down into the substrate than in the substrate introduced and/or present PN-junctions.

3. A semiconductor component arranged at a surface of a substrate, **characterized by** a multitude of plugs, extending from the inner of the substrate to the surface of the semiconductor component for electrical shielding of the semiconductor component.

4. A component according to claim 3, **characterized in** that the plugs extend deeper down into the substrate than in the substrate introduced and/or present PN-junctions.

5. A component according to any of claims 3 or 4, **characteriz d in** that the upper ends of the plugs are interconnected by means of an electrically conducting material, in particular a material having a good electrical conductivity, in particular a metal material.

6. A method of manufacturing a semiconductor component having a substrate connection comprising that the semiconductor compon nt is manufactured in and/or at a surface of the substrate, **charact rized by** the further steps of:
- making at least one hole from the surface on or next to the semic nductor component down into the underlying substrate, preferably d ep down into the substrate, and
- thereupon filling said hole with metal.

7. A method according to claim 6, **characterized in** that the hole is made deeper down into the substrate than in the substrate introduced and/or present PN-junctions.

8. A method of manufacturing a semiconductor component having a substrate connection comprising process steps for obtaining the different parts of the semiconductor component in and/or at a surface of the substrate, one process step comprising that contact holes are filled with an electrically conducting material, in particular a material having a good electrical conductivity, in particular a metal material, for obtaining contact with areas in the semiconductor component, **characterized by** the further step of, before the filling of the contact holes, making a hole from the surface at or next to the semiconductor component down into the underlying substrate, preferably deep down into the substrate.

9. A method according to claim 8, **characterized in** that said hole is made having a diameter or largest across-corner dimension, which essentially corresponds to corresponding measures for the contact holes, and/or are so chosen that the hole is filled in the process step for filling the contact holes.

10. A method of manufacturing a semiconductor component or group of semiconductor components electrically shielded against surrounding components, **characterized in**
- that a multitude of holes are made deep down into an underlying substrate around the whole or parts of said semiconductor component and/or group of semiconductor components and
- that said hole are filled with metal.

11. A method according to claim 10, **charact riz d in** that the holes are made deeper down into the substrate than in the substrate introduced and/or present PN-junctions.

12. A method according to any of claims 10 or 11, **characterized in** that the upper ends of the metal-filled holes are connected

by an electrically conducting material.

13. A shielded electrical signal conductor in a semiconductor structure, **characterized in** that plugs of metal are arranged along the sides of the signal conductor and that said plugs of metal are arranged so close that a good lateral shielding of the electrical signal conductor is obtained.

14. A signal conductor according to claim 13, **characterized in** that the signal conductor also is shielded in a vertical direction by means of metal planes provided in the semiconductor structure.

15. A method of manufacturing a shielded electrical signal conductor in a semiconductor structure, **characterized in**
- that holes are made at the side of the electrical signal conductor,
- that said holes are located close next to each other and
- that the holes then are filled with metal.

16. A method according to claim 15, in the case when the electrical signal conductor is shielded in a vertical direction by one or several metal planes, **characterized in** that the holes are made so deep that they at least reach down to a metal plane located closest underneath the electrical signal conductor.

17. A semiconductor component arranged at the surface of a substrate comprising an electrical connection between the substrate and the surface on and/or at the semiconductor component, **characterized in** that the connection comprises a plug of a material having a good electrical conductivity, in particular a material of another type than the substrate, in particular a metal plug, which extends between the inner of the substrate and the surface layer at or on the semiconductor component and that on top of the component there is provided a layer of an electrically conducting material, in particular a m tal.

18. A semiconductor component according to claim 17, **characterized in** that the electrically conducting layer is grounded.

19. A semiconductor component arranged at the surface of a substrate, **characterized by** a multitude of plugs, which extend between the inner of the substrate and the surface at the semiconductor component for electrical shielding of the semiconductor component and that on top of the component there is provided a layer of an electrically conducting material, in particular a metal.

20. A semiconductor component according to claim 17, **characterized in** that the electrically conducting layer is grounded.

21. A method of manufacturing a semiconductor component or a group of semiconductor components electrically shielded against surrounding components, **characterized in**
- that a multitude of holes are made deep down into an underlying substrate around the whole or parts of said semiconductor component and/or group of semiconductor components and
- that said holes are filled with metal, and
- that a layer of an electrically conducting material, in particular a metal is provided on top of the semiconductor component or group of semiconductor components.

22. A method according to claim 21, **characterized in** that the electrically conducting layer is grounded.

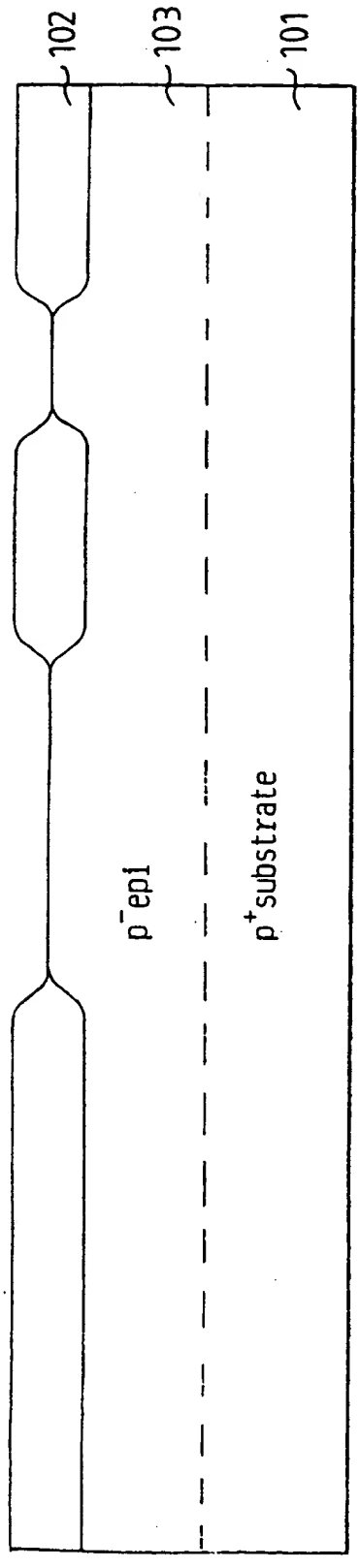
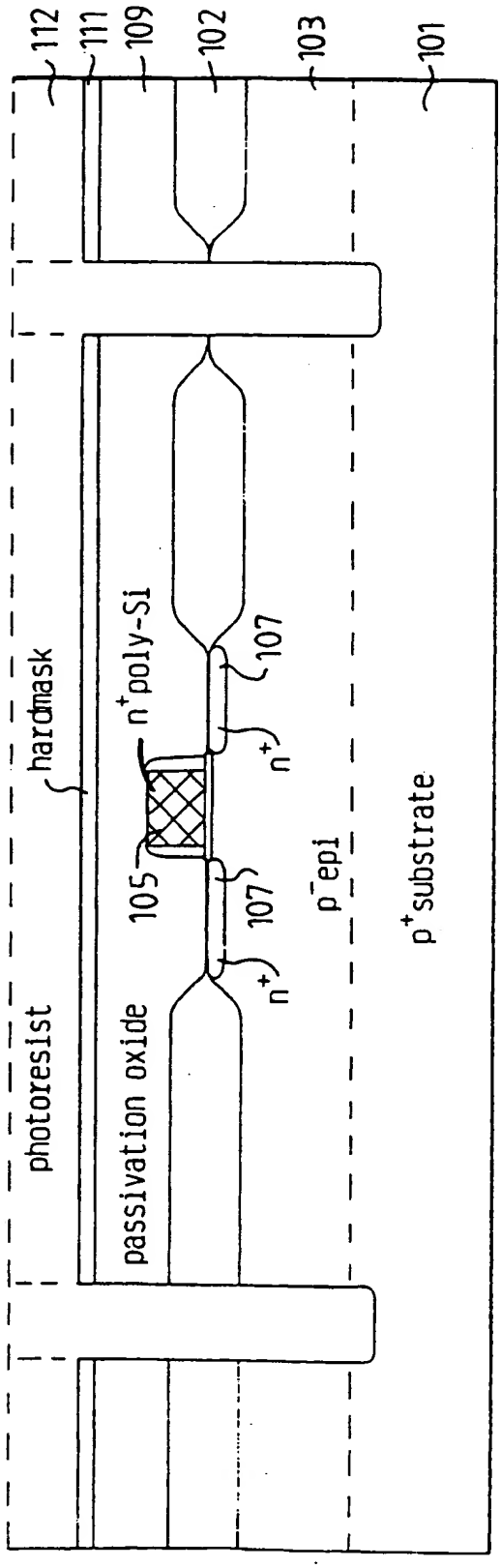

102
103
101
p⁻epi
p⁺substrate

FIG.1a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111
109
102
103
101
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107
n⁺
105
107
n⁺
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passivation oxide
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p⁺substrate

FIG.1b

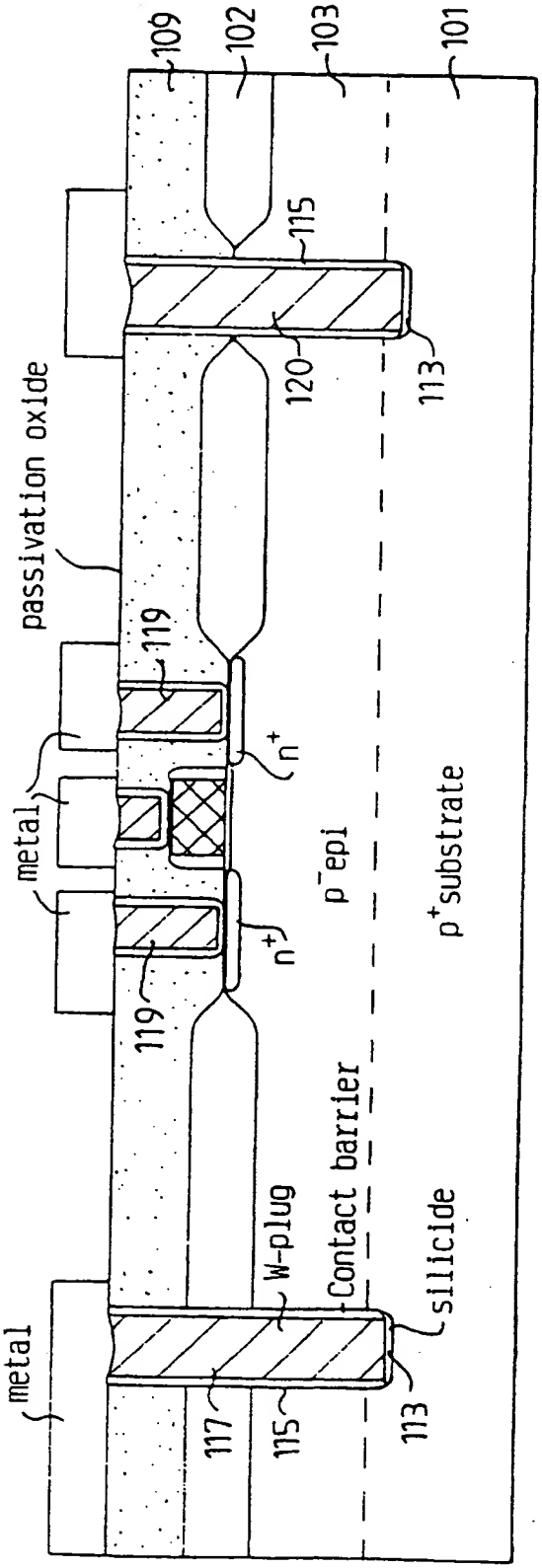
109
102
103
101
115
120
113
passivation oxide
119
n+
metal
p- epi
p+ substrate
n+
119
Contact barrier
W-plug
silicide
metal
117
115
113

FIG. 1c

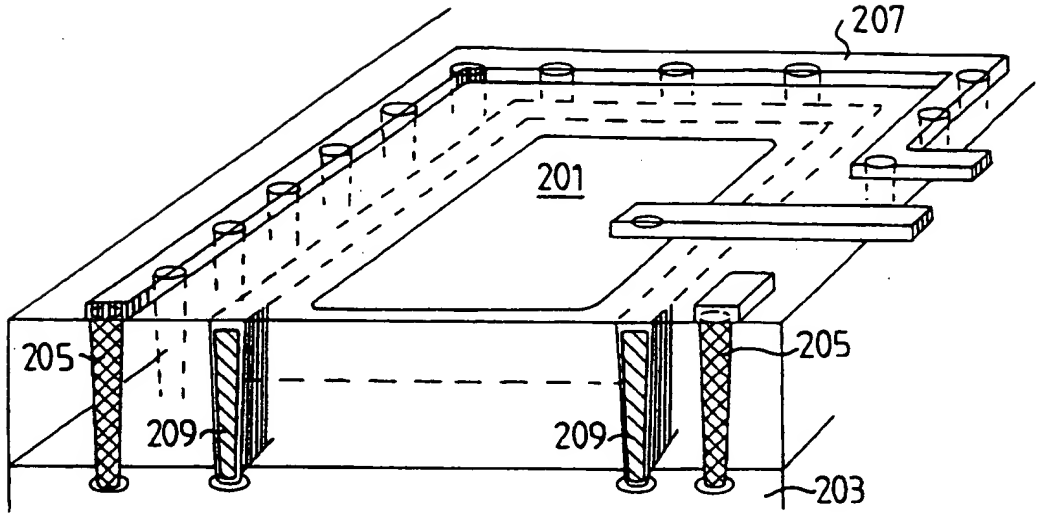

FIG. 2

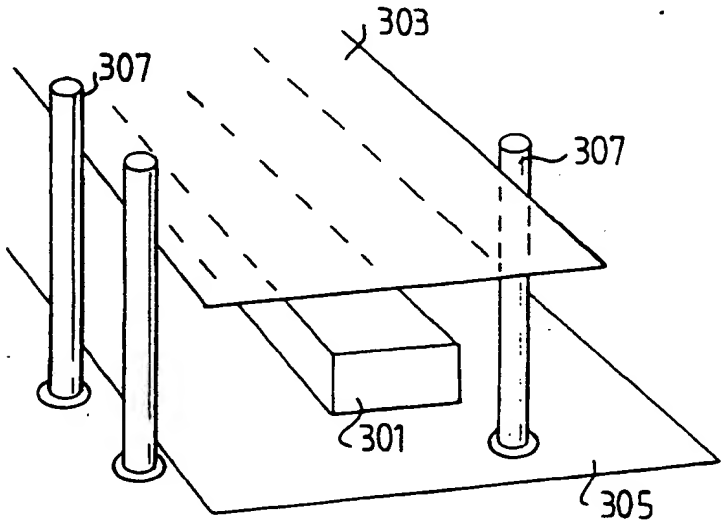

FIG. 3

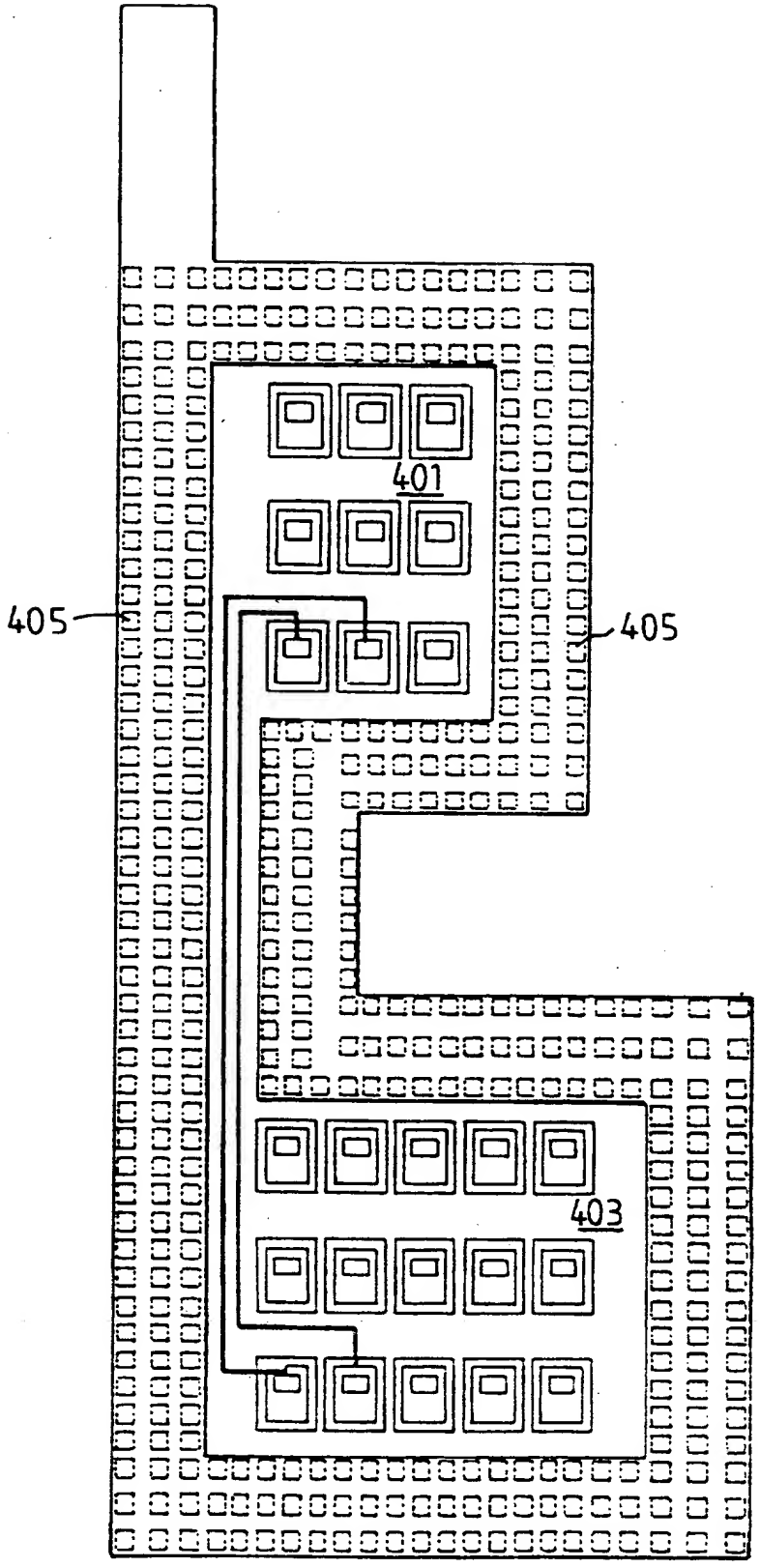

FIG. 4

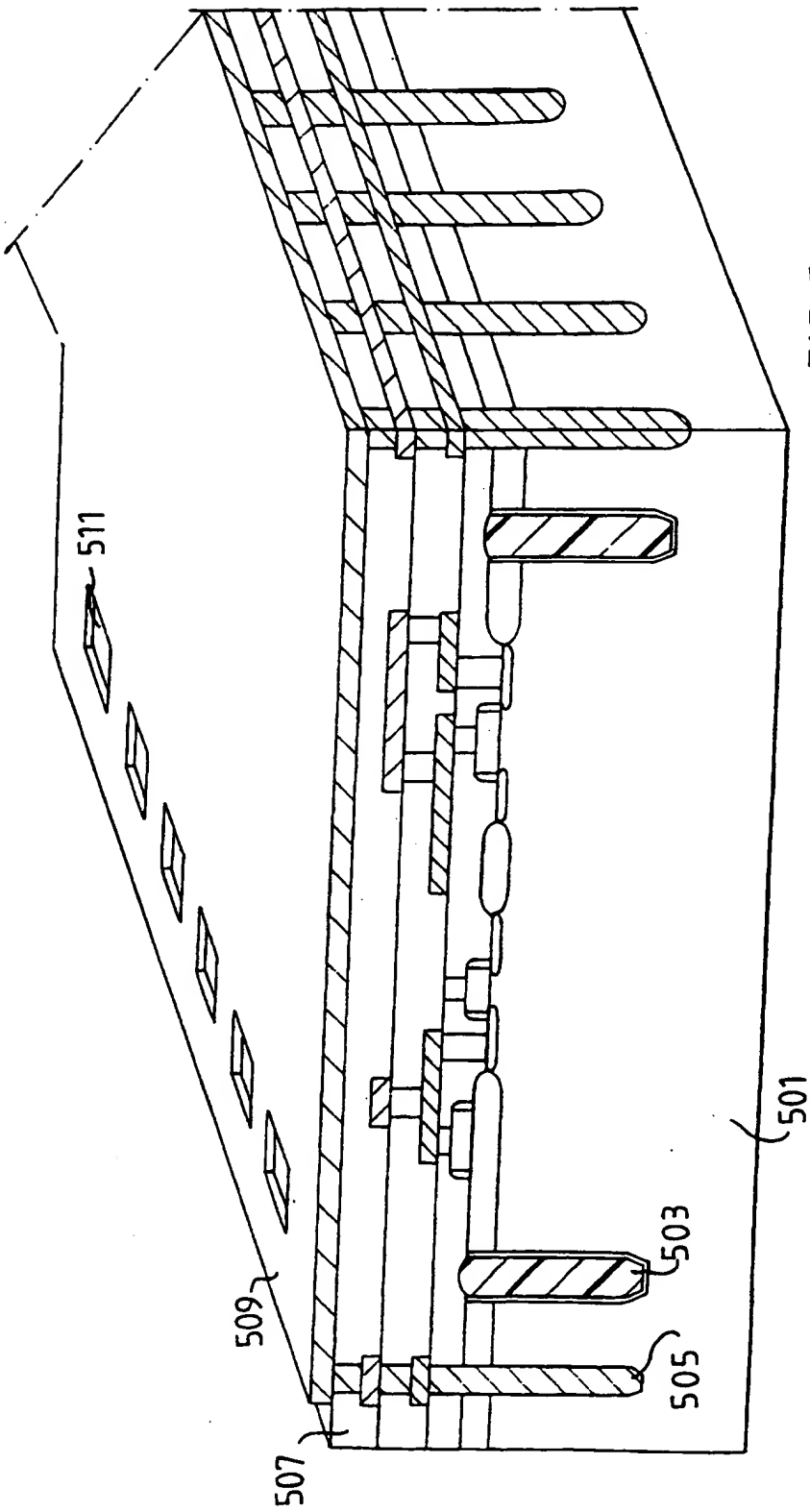

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 97/00487

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 23/60, H01L 23/52, H01L 21/28
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: 350,351

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5151770 A (A. INOUE), 29 Sept 1992 (29.09.92), column 4, line 22 - column 5, line 49; column 6, line 55 - column 9, line 20, figures 1-5, claims 1-9	1-22
X	Patent Abstracts of Japan, Vol 16,No 116, E-1181, abstract of JP,A,32-86559 (MITSUBISHI ELECTRIC CORP), 17 December 1991 (17.12.91)	1-22
A	US 5288949 A (H.S. CRAFTS), 22 February 1994 (22.02.94), figures 1-11, abstract	1-22

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
7 August 1997	11 -08- 1997
Name and mailing address of the ISA/ Swedish Patent Office	Authorized officer

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 97/00487

C (C ntinuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim N .
A	EP 0567694 A1 (MITSUBISHI DENKI KABUSHIKI KAISHA), 3 November 1993 (03.11.93), figures 1,2, abstract --	1-22
A	US 4958222 A (H. TAKAKURA ET AL.), 18 Sept 1990 (18.09.90), column 1, line 57 - column 2, line 2, figures 1-12 --	1-22
A	Patent Abstracts of Japan, Vol 12,No 489, E-696, abstract of JP,A,63-202941 (NEC CORP), 22 August 1988 (22.08.88) --	13-16
A	Patent Abstracts of Japan, Vol 7,No 140, E-182, abstract of JP,A,58-54661 (FUJITSU KK), 31 March 1983 (31.03.83) --	13-16

INTERNATIONAL SEARCH REPORT

Information on patent family members

01/07/97

International application No.
PCT/SE 97/00487

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5151770 A	29/09/92	GB 2238911 A,B	12/06/91
		JP 3165058 A	17/07/91
		US 5256590 A	26/10/93
US 5288949 A	22/02/94	JP 5343601 A	24/12/93
EP 0567694 A1	03/11/93	US 5196920 A	23/03/93
US 4958222 A	18/09/90	EP 0353426 A	07/02/90
		JP 2001928 A	08/01/90